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EXAMINER	
CHANDRASEKHAR, PRANAV	

ART UNIT	PAPER NUMBER
2115	2

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,180	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 16 is objected to because of the following informalities:

In line 3 of claim 16, the word has been 'implemented' has been misspelled as 'implements'.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,4-6,10,11 and 14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kanuma [US Pat No. 4,587,445].

3. As per claim 1, Kanuma teaches

a unit for counting the logic state transitions on the bus during a period of time [col. 3 lines 33-51. The majority circuit is viewed as containing a unit for counting the number of logic state transitions since it generates a control signal depending on the number of logic state transitions.]; wherein the bus power consumption is determined by the number of logic state transitions [col. 1 lines 39-43; col. 5 lines 7-27. A renewal of logic data is manifested as a transition from one logic state to another. The power consumed on the power source line is directly proportional to the noise voltage

generated as a result of the logic state transition. Hence, the bus power consumption is determined by the number of logic state transitions].

4. As per claim 2, Kanuma teaches

a storage component, the storage component storing on the output terminal a first signal [col. 1 lines 13-27; T1-TN Fig 2. The signals T1-TN are viewed as being stored on a storage component prior to being transmitted across the bus.] representative of a logic state of the coupled bus conductor [The storage component containing logic date T1 is coupled to the bus conductor via the logic gate 20-1, D-type flip flop 22-1 and output buffer 24-1 to the bus conductor L1.];

a delay component coupled to the output terminal of the storage unit [22-1 – 22-N Fig 2], the output terminal of the delay component storing the logic state of the delayed signal, the delayed signal being the first signal delayed by a clock cycle [col. 2 lines 49-53; col. 3 lines 55-61; col. 4 lines 15-20. The output signal is the logic state of the first signal in the previous clock cycle and hence is a delay of the first signal]; and

a difference component coupled to the output terminal of the storage component and the output terminal of the delay component, the difference component is a logic element capable of detecting a difference in consecutive bus states [28-1 – 28-N Fig 2; col. 3 lines 33-47. The logic state as defined by signal T1-TN is representative of the logic state of the signal in the present clock cycle and the output of each D-type flip flop is representative of the signal state in the previous clock cycle. Hence, the difference component compares consecutive bus states and generates a non-coincident signal (result signal) if there is a difference of logic state in consecutive clock cycles.].

5. As per claim 4, Kanuma further teaches the difference component to be ab "exclusive OR" logic gate [col. 3 lines 42-47].

6. As per claim 5, Kanuma further teaches

a count logic component coupled to all of the difference components, the count logic component determining the number of result signals during each clock cycle [col. 2 line 62 – col. 3 line 1. The majority circuit is viewed as containing a count logic unit coupled to all of the difference components since it generates a control signal in based on the number of non-coincident signals (result signals)] and

an adder component coupled to the count logic component, the adder component summing the number of result signals generated during each clock cycle and storing the count of result signals [col. 2 line 62- col. 3 line 1. The majority circuit is viewed as containing an adder component since it generates a control signal based on the number of non-coincident signals (result signals)].

7. As per claim 6, Kanuma further teaches the count of result signals to be the count of total number of transitions [col. 3 lines 47-51].

8.As per claim 10, Kanuma teaches

measuring the number of logic transitions of the bus during a period [col. 3 lines 33-51. The majority circuit is viewed as containing a unit for counting the number of logic state transitions since it generates a control signal depending on the number of logic state transitions.], each logic signal transition consuming power [col. 1 lines 39-43; col. 2 lines 49-53; col. 5 lines 7-27. A renewal of logic data from one clock cycle to the next is manifested as a transition from one logic state to another. The power consumed

on the power source line is directly proportional to the noise voltage generated as a result of the logic state transition. Hence, the bus power consumption is caused by logic state transitions].

9. As per claim 11, Kanuma teaches

comparing the state of a logic signal on each bus conductor during a first clock cycle with the state of the logic signal on the same bus conductor during the next sequential clock cycle 28-1 – 28-N Fig 2; col. 3 lines 33-47. The logic state as defined by signal T1-TN is representative of the logic state of the signal in the present clock cycle and the output of each D-type flip flop is representative of signal in the previous clock cycle. Hence, the difference component compares consecutive bus states and generates a non-coincident signal (count signal) if there is a difference of logic state in consecutive clock cycles.];

generating a count signal when the state of a logic signal on a bus conductor is different during a second clock period that the state of the logic signal on the same bus conductor during the first clock period [col. 3 lines 42-47]; and

during the period, determining the total number of count signals [col. 3 lines 47-51; col. 2 lines 49-53].

10. As per claim 14, Kanuma teaches

a plurality of temporary storage components, each temporary storage component coupled to a conductor of the internal bus, each temporary storage component applying the logic state signal to an output terminal [T1-TN Fig 2; col. 1 lines

13-27. The signals T1-TN are viewed as being stored on a storage component prior to being transmitted across the bus.]

a plurality of delay components, each delay component having an input terminal coupled to the output terminal of a temporary storage, the delay unit applying the logic state signal applied to the output terminal of the coupled temporary storage component during the next sequential clock cycle [22-1 – 22-N Fig 2; col. 2 lines 49-53; col. 3 lines 55-61; col. 4 lines 15-20. The output signal of the delay element is the logic state of the first signal that is stored in the corresponding storage component and is hence applied during the next sequential clock cycle];

a plurality of difference components [28-1 – 28-N Fig 2], a first input terminal of each difference component coupled to an output terminal of a temporary storage component, a second input terminal of the difference component coupled to the output terminal of the temporary storage component coupled to the first input terminal, each difference component providing difference signal when the signal applied to the first input terminal of the difference components is not the same as the signal applied to the second input terminal of the difference component [col. 3 lines 33-47];

a count component having the output terminal of the difference components applied thereto, the count component determining the number of difference signals [col. 2 line 62-col. 3 line 1. The majority circuit is viewed as containing a count logic unit coupled to all of the difference components since it generates a control signal in response to the number of non-coincident signals (difference signals)]; and

an adder unit coupled to the count component for adding the number of difference signals determined for each clock cycle, the number of difference signals being an indicia of the power consumed [col. 2 line 62-col. 3 line 1;col. 5 lines 7-27. The majority circuit is viewed as containing an adder unit coupled to the count component since it triggers a control signal based on the number of non-coincident signals (difference signals).].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3,7-9,12,13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma [US Pat No. 4,587,445].

12. As per claim 3, Kanuma further teaches the delay component to be latch/flip-flop components [col. 3 lines 55-61] and the difference component to be a logic element capable of detecting a difference in consecutive bus states [28-1 – 28-N Fig 2; col. 3 lines 33-47. The logic state as defined by signal T1-TN is representative of the logic state of the signal in the present clock cycle and the output of each D-type flip flop is representative of signal in the previous clock cycle. Hence, the difference component

compares consecutive bus states and generates a non-coincident signal (result signal) if there is a difference of logic state in consecutive clock cycles.].

Kanuma does not explicitly teach the storage component to be a latch/flip-flop component.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to use a latch/flip-flop circuit to store the logic state of the first signal prior to being transferred on the bus conductor since latches and flip-flops are commonly used storage elements that are well known in the art.

13. As per claim 7, Kanuma does not explicitly teach a trigger component, wherein the trigger component is responsive to control signals for activating the count of bus logic state transitions.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a trigger component that is responsive to control signals for activating the count of bus logic state transitions since it would be advantageous for the count unit to receive an indication of when it must begin counting the number of bus logic state transitions.

14. As per claim 8, Kanuma does not explicitly teach the control signals determining whether the trigger component activates the count of bus logic state transitions during activity of an internal bus, during activity of an external bus, during activity of both the internal and external bus, or during a preselected window of the software activity.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a trigger component to activate the count of bus logic state transitions during specific activities (such as internal bus activity and external bus activity) since it would be advantageous to provide a method by which transitions during specific times and specific buses may me monitored.

15. As per claim 9, Kanuma does not explicitly teach a plurality of adder components, each adder component determining bus logic transitions in response to control signals from the trigger unit.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a plurality of adder components that determine bus logic transitions in response to control signals from the trigger unit since it would be advantageous to count the number of bus logic transitions during specific periods as dictated by the control signals.

16. As per claim 12, Kanuma does not explicitly teach determining the total number of count signals for an external bus in response to a second control signal.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to determine total number of count signals for an external bus in response to a second control signal in a manner similar to that of determining number of count signals for an internal bus since it would be advantageous to monitor number of logic transitions on an external bus and accordingly determine the power consumption in the external bus.

17. As per claim 13, Kanuma does not explicitly teach a second control signal triggering the determination of the total number of count signals for an internal bus.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a second control signal to trigger the determination of the total number of count signals for an internal bus since it would be advantageous for the count circuit to receive an indication of when it must determine the number of count signals for an internal bus.

18. As per claim 15, Kanuma does not explicitly teach the adder unit being activated for a period of time.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to enable the adder unit to activated for a period of time since it would be advantageous to count number of logic state transitions within a specific time frame and thus determine the power consumption in that time frame.

19. As per claim 16, Kanuma further teaches

the delay component being implemented with latch/flip-flop components [col. 3 lines 55-61; 22-1 – 22-N Fig 2] and the difference components are implemented with "exclusive OR" logic components [28-1 – 28-N Fig 2; col. 3 lines 33-47.],

Kanuma does not explicitly teach the storage components to be a latch/flip-flop components.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to use latch/flip-flop circuits to store the logic states of the first signal prior to

being transferred on the bus conductors since latches and flip-flops are commonly used storage elements that are well known in the art.

20. As per claim 17, Kanuma does not explicitly teach a trigger unit coupled to the adder component, the trigger unit responsive to first control signals or activating the adder component for a period of time.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a trigger unit coupled to the adder component, the trigger unit being responsive to first control signals for activating the adder component for a period of time in order to monitor the number of logic state transitions for a specific period of time as indicated by the trigger component.

21. As per claim 18, Kanuma does not explicitly teach the buffer unit being coupled to an external bus, the trigger unit responsive to second control signals for measuring the difference signals on the external bus.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to measure the difference signals on an external bus one being triggered by a trigger unit with second control signals in a manner similar to that of measuring difference signals on an internal bus.

22. As per claim 19, Kanuma does not explicitly teach a plurality of adder components, each adder component activated by control signals from the trigger unit.

It would have been obvious to one skilled in the art to modify the teachings of Kanuma to incorporate a plurality of adder components each of which is activated by control signals from the trigger unit since it would be advantageous to include the option

of monitoring logic state transitions during specific periods of time as dictated by the control signal from the trigger unit.

Conclusion

23. An examination of this application reveals that applicant is unfamiliar with patent prosecution procedure. While an inventor may prosecute the application, lack of skill in this field usually acts as a liability in affording the maximum protection for the invention disclosed. Applicant is advised to secure the services of a registered patent attorney or agent to prosecute the application, since the value of a patent is largely dependent upon skilled preparation and prosecution. The Office cannot aid in selecting an attorney or agent.

Applicant is advised of the availability of the publication "Attorneys and Agents Registered to Practice Before the U.S. Patent and Trademark Office." This publication is for sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached between 8:30 a.m. – 5:00p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar

April 16,2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100